Since the dry process identified in the invention process predominately affects only the surfaces of polycrystalline CdTe, the disadvantageous grain-boundary etching of the polycrystalline CdTe shown in Figure 7b is avoided as a result of using the dry process of the present invention (see paragraph bridging pages 11 and 12 of the specification).

It is believed that these discussions have materially advanced the prosecution of this application.

The Official Action and the cited references have again been carefully reviewed. The review indicates that the claims, especially as amended, recite patentable subject matter and should be allowed. Reconsideration and allowance are therefore respectfully requested.

Prior to contending with the grounds upon which the rejections are based, it is useful to summarize the essentials of the invention "dry process" for providing uniform and reproducible low-resistance electrical contacts (page 15, lines 15-19) between a metal and a layer of polycrystalline p-type CdTe surface of a semiconductor device by an argon beam of Ar atoms prior to forming a contact interface or additional semiconductor layer.

Applicant is the first to invent a "dry process" for making a uniform and reproducible surface of low-resistance electrical contact between a metal and a layer of polycrystalline p-type CdTe surface through the use of a unique form of Ar ion beam processing prior to forming a contact interface or additional semiconductor layer.

The invention process is accomplished by:

a) placing a CDs/CdTe device having a polycrystalline p-type CdTe into a chamber and evacuating the chamber to create a vacuum;

b) orientating the polycrystalline p-CdTe side of the CDs/CdTe device to face apparatus capable of generating Ar atoms and ions of preferred energy and directionality;

c) introducing Argon and igniting the area of apparatus to generate Ar atoms and ions of preferred energy and directionality in a manner so that during ion exposure, the source-to-substrate distance is maintained such that it is less than the mean-free path or diffusion length of the Ar atoms and ions at the vacuum pressure; and

d) allowing exposure of the polycrystalline p-CdTe side of the layer to the ion beam for a period less than about 5 minutes prior to forming a contact interface or additional semiconductor layer.

Claims 1-2 and 4 were rejected as being unpatentable over admitted prior art in combination with Schroen et al. under 35 U.S.C. §103(a).

Applicant respectfully traverses the rejection and requests reconsideration for the following reasons.

While the "admitted prior art" on pages 5 and 6 of applicant's specification disclose methods of making CdS/CdTe devices, these processes clearly lack teaching a "dry process" for providing a uniform and reproducible surface of low-resistance electrical contact between a metal and a layer of polycrystalline p-type CdTe surface of a semiconductor, let alone suggesting, teaching or disclosing exposing a polycrystalline p-type CdTe to Ar ions or atoms prior to forming an additional contact interface or semiconductor layer to reduce contact resistance.

The deficiencies of these "admitted prior art" references are not compensated for by any teachings or disclosure in the secondary reference of Schroen et al.

Schroen et al. is directed to a process for fabrication of a semiconductor ohmic contact structure comprising:

a. exposing a selected portion of a semiconductor body to a glow discharge in the presence of an inert gas;

b. exposing the selected portion to a glow discharge in oxygen or nitrogen, at conditions selected to form an adherent uniform film of nonconductor 10-100 Angstroms thick on the selected portion of the semiconductor body; and

c. forming an adherent film of conductor on the nonconductor film, to complete a contact structure having linear I-V characteristics.

The Schroen et al. patent deals with crystalline Si, and not a polycrystalline CdTe.

Further, the only specific material on which the process of Schroen et al. has been demonstrated is crystalline Si. However, Si forms a stable oxide and this oxide is non-reactive with most metals.

Significantly, Schroen et al. discloses the use of a "glow discharge in the presence of an inert gas" specifically to activate the Si surface for a subsequent formation of "an adherent uniform film of non conductor".

By contrast, applicant's invention is directed to use of an ion-beam process to condition a polycrystalline p-CdTe surface prior to deposition of an additional semiconductor layer. Consequently, the invention process is not conditioning the surface to facilitate formation of a non conductor - but rather a semiconductor.

Moreover, the ion dynamics and the plasma chemistry occurring in the surface of the clean crystalline Si, and caused by exposure to a 1-10keV glow discharge of Schroen et al., which is high-voltage, high-pressure is vastly different from the 0.05-2keV ion-beam exposure (low-voltage, low-pressure) of the $CdCl_2$-treated polycrystalline p-CdTe of the invention process.

The improvement in the interfacial current transport at the p-CdTe interface of the invention is by improved alignment of the valence bands between semiconductors. By contrast, the improvement in current transport of the Si/oxide/metal interface of Schroen et al. is by the creation of "a semiconductor-insulator interface with suitable electrical properties to create an accumulation in the adjacent semiconductor."

Thus, even if the "accumulation layer" would improve quantum-mechanical tunneling between a semiconductor and a metal, it nevertheless represents very different physics of interfacial current transport, and the process used to provide optimal "activation" of a Si surface is drastically different than the invention process which is used to prepare the surface of a polycrystalline p-CdTe film.

Therefore, the combination of Schroen et al. with "admitted prior art" cannot be reconciled under the provisions of 35 U.S.C. §103 for purposes of rendering claims 1-2 and 4, especially as amended, obvious.

Withdrawal of the rejection is respectfully requested.

Claim 5 has been rejected as being unpatentable over "admitted prior art" in combination with Schroen et al., further in view of Lee et al. under 35 U.S.C. §103(a).

Applicant respectfully traverses the rejection and requests reconsideration for the following reasons.

The "admitted prior art" and Schroen et al. have already been discussed above.

The collective deficiencies in the "admitted prior art" and Schroen et al. are not compensated for in the teachings of the Lee et al. reference.

This is so because Lee et al. is directed to an external plasma gun that provides both ions and electrons for bombarding substrates. There is no reference to or acknowledgment of the use of this external plasma gun to condition a polycrystalline p-CdTe surface prior to deposition of an additional semiconductor layer. Therefore, the fact that an exit aperture having a diameter of 3cm is disclosed would provide no incentive for or reason why one skilled in the art would be led to utilize this external plasma gun with an aperture of 3cm in one of its specific embodiments for use as an ion-beam in combination with Schroen et al. and the "admitted prior art" to condition a polycrystalline p-CdTe surface prior to deposition of an additional semiconductor layer.

Withdrawal of the rejection is respectfully requested.

Claim 6 was rejected as being unpatentable over "admitted prior art" in combination with Schroen et al., further in view of Ebe et al., under 35 U.S.C. §103(a).

Applicant respectfully traverses the rejection and requests reconsideration for the reasons hereinafter explained.

All of the "admitted prior art" and Schroen et al. have been discussed supra.

Ebe et al. is directed to a method for manufacturing film carrier type substrates in a vacuum by depositing a metal vapor on a file made of organic high molecular substance and irradiating accelerated nitrogen gas ions on the film simultaneously with the step of depositing metal vapor.

Ebe et al.'s teachings clearly are non-related to those of the "admitted prior art" and Schroen et al. for the reason that Ebe et al. is directed to providing a carrier type substrate that includes the film of organic high molecular weight substance and a metal formed thereon to effect high density mounting of integrated circuits to obtain super-adhesive characteristics. Therefore, there would be no incentive or reason why one skilled in the art of making CDs/CdTe devices by conditioning a

polycrystalline p-CdTe surface prior to deposition of an additional semiconductor layer by looking to the art of obtaining super adhesion between an organic high molecular weight substance and a metal layer formed thereover and an appropriate exposure angle of an ion beam source for making a uniform and reproducible surface of a low-resistance electrical contact between a metal and a layer of polycrystalline p-type CdTe surface.

Thus, the combination of "admitted prior art" with Schroen et al. and Ebe et al. cannot be reconciled under the auspices under 35 U.S.C. §103 for rejecting claim 6 as presently recited.

In view of the foregoing amendments, remarks and arguments, it is believed that the application is now in condition for allowance, and early notification of the same is earnestly solicited.

Respectfully submitted,

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